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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,432	02/06/2004	Toshiki Kaneko	501.43456X00	6107

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EXAMINER	
WARREN, MATTHEW E	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/772,432	KANEKO ET AL.	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,13 and 14* is/are rejected.

7)☒ Claim(s) *11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/6/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Preliminary Amendment filed on March 5, 2004.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

Claim 9 is objected to because of the following informalities: In the second line of the claim, "pure No" should be "pure Mo."

Claim 13 is objected to because of the following informalities: The second line of the claim contains the limitation of "...the semiconductor layer." There is insufficient antecedent basis for this limitation in the claim. Also, in the last line of the claim the limitation of "the LCD region" should be LDD region. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4-9, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. (US 6,255,706 B1) in view of Shimomaki et al. (US 6,678,017 B1).

In re claims 1, 4, and 7, Watanabe et al. shows (figs. 4B-6C)a display device having thin film transistors on a substrate thereof, wherein the display device includes gate patterns in each of which a gate line and a gate electrode of the thin film transistor are integrally formed, and drain lines (col. 3, lines 4-57); an insulation film (51) covers the gate pattern (as shown in the more complete embodiment of fig. 5A); the gate pattern (40) is constituted by at least three-layered films consisting of a lowermost layer (5), an intermediate layer (6) formed of at least one layer and an uppermost layer (7) at least at either a portion of the thin film transistor or a portion of the gate pattern which crosses a drain line, the intermediate layer is formed of a material selected from the group consisting of pure Al, an Al alloy, pure Ag, an Ag alloy, pure Cu and a Cu alloy (col. 6, lines 48-67), and the uppermost layer and the lowermost layer are formed of a metal (Mo) having a melting point higher than the melting point of the material of the intermediate layer. The uppermost and lowermost layers are formed of a Mo alloy. The Mo alloy inherently has a higher melting point than that of Al because the materials of and structure of the three layers is the same as the applicant's claimed invention. Watanabe shows all of the elements of the claims except the end portions of the intermediate layer recessed from end portions of the uppermost layer and end portions of the lowermost layer. Shimomaki et al. shows (fig. 10B) a display device having a three layered gate pattern wherein end portions of an uppermost layer (104a) of the

gate electrode are spaced inwardly from end portions of the lowermost layer (102) and at the same time, end portions of the intermediate layer (103) are recessed from end portions of the uppermost layer and end portions of the lowermost layer. With this configuration, the reliability of the gate is improved because no electromotive force is generated in the overhang portions(col. 12, lines 24-61). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the gate electrode of Watanabe by forming the intermediate layer having end portions recessed from end portions of the uppermost and lowermost layer as taught by Shimomaki to eliminate electromotive force in the upper level overhang and ultimately improve reliability of the structure.

In re claim 2, Watanabe discloses that the uppermost and lowermost layers are formed of a Mo alloy (col. 6, lines 48-67).

In re claims 5, 6, and 14, Watanabe shows (fig. 5A) the thin film transistor including a semiconductor layer (52) but does not disclose that the layer includes a polycrystalline semiconductor. However, polycrystalline is well known in the art for use as a semiconductor layer in a TFT.

Claims 3 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. (US 6,255,706 B1) in view of Shimomaki et al. (US 6,678,017 B1) as applied to claims 1 and 7 above, and further in view of Jeong et al. (US 6,081,308).

In re claim 3 and 10, Watanabe and Shimomaki show all of the elements of the claims except the uppermost and lowermost layers formed of a Mo-W alloy. Jeong et al.

discloses (col. 9, lines 57-67) a multi-layered gate line for an LCD that uses a Mo-W alloy for the upper layer. The Mo-W alloy prevents hillock formation in the Al layer and reduces the number of lithography steps (col. 12, lines 52-65). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the uppermost and lowermost layers of the gate electrode of Watanabe and Shimomaki by using Mo-W as taught by Jeong to prevent hillock formation in the Al and reduce the processing steps.

Claims 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. (US 6,255,706 B1) in view of Shimomaki et al. (US 6,678,017 B1) as applied to claim 7 above, and further in view of Jinno et al. (US Pub. 2001/0005020 A1).

In re claim 13, Watanabe and Shimomaki show all of the elements of the claims except the semiconductor layer including an LDD and a portion of the gate that overlaps the LDD region. Jinno et al. shows (fig. 5) a TFT for a display in which LDD regions (82a and 83a) are formed in a semiconductor layer and overlap portions of the gate electrode (76) to increase the OFF resistance of the TFT [0032]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor layer of Watanabe and Shimomaki by adding LDD regions as taught by Jinno to increase the OFF resistance of the TFT.

Allowable Subject Matter

Claims 11 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Whetten (US 5,153,754), Takahashi et al. (US 6,731,364 B2), and Kaneko et al. (US Pub. 2001/0030717 A1) also show display devices having multilayered gate electrodes.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW
MEW
June 22, 2005

Tom Thomas
TOM THOMAS
SUPERVISORY PATENT EXAMINER